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09/737,375	12/14/2000	Mario Nemirovsky	P3808	1798

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EXAMINER

SEFCHECK, GREGORY B

ART UNIT	PAPER NUMBER
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2662

DATE MAILED: 04/05/2004

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/737,375

Applicant(s)

NEMIROVSKY ET AL.

Examiner

Gregory B Sefcheck

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-59 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-7, 9, 10, 13-16, 18-26, 28, 29, 32-35, 37-45, 47, 48, 51-54, 56, 59 is/are rejected.
- 7) ☒ Claim(s) 8, 11, 12, 17, 27, 30, 31, 36, 46, 49, 50 and 55 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 April 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 4, 5, 6.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed 10/21/2003 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

Examiner notes that a total of three IDS were filed. Only the IDS filed on 10/21/2003 was received without copies of the references. The other two IDS, filed on 7/24/2002 and 3/5/2004, were received with proper copies.

Claim Objections

2. Claims 52 and 55 are objected to because of the following informalities:

- Claims 52 and 55 improperly depend from claims 13 and 8, respectively. Claims 52 and 55 appear to properly depend from claims 51 and 46, respectively.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 59 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- In regards to Claim 59,

The use of a probe bit associated with each packet for ensuring that a packet number assigned to a packet at one point in time is assigned to the same packet at another point in time is indefinite. It is unclear how asserting the probe bit through a Probe&Set command by a stream indicates that the assigned packet number is associated with the same packet.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

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6. Claims 1, 4, 6, 7, 9, 15, 16, 18, 20, 23, 25, 26, 28, 34, 35, 37, 39, 42, 44, 45, 47, 53, 54, 56, 58, and 59 are rejected under 35 U.S.C. 102(e) as being anticipated by Muller et al. (US006483804B1), hereafter Muller.

- In regards to Claims 1, 4, 20, 23, 39, and 42,

Muller discloses a method and system for queuing packets identified by data flow to be collectively processed (Abstract; claim 1/20/39 – configurable queuing system/method in a data packet processor).

Referring to Figs. 8, 9, 10, 21, and 24, Muller shows a plurality of queues arranged in several elements of the processing system (claim 1/20/39 – plurality of queues arranged in one or more clusters). Muller shows the plurality of queues capable of storing information associated with 256 packets (Fig. 8 & 9; claim 4/23/42 – total number of packet identifiers is 256, allowing 256 packets in process at one time). Muller shows packets are sent to packet queue 116 as packet identifiers are generated (Col. 8, lines 40-43; claim 20 – processor has input buffer, local packet memory and stream processor).

Referring to Figs. 1A, Muller shows logic that generates identifiers for each arriving packet (Col. 8-9, lines 50-17; claim 1/20/39 – identification mechanism for creating packet identifier for arriving packets).

Muller further shows logic for associating the identifiers of each packet with the associated plurality of queues (Col. 9-10, lines 42-13; Col. 52-54, lines 5-32; claim 1/20/39 – insertion logic for determining and inserting packet identifiers into queues).

Muller shows DMA 120 selects the packet identifiers for processing (Col. 54, lines 32-65; claim 1/20/39 – selection logic for selecting packet identifiers from queues to initiate processing, downloading or requeueing).

- In regards to Claims 6, 25, and 44,

Muller discloses a method and system for queuing packets identified by data flow to be collectively processed that covers all limitations of the parent claims.

Muller shows that the packet identifiers of arriving packets are associated with the memory location where the packet is to be stored when selected for transfer by the DMA 120 (Col. 54, lines 47-65; claim 6/25/44 – packet identifier created is associated to a memory location where the packet itself is stored during processing).

- In regards to Claims 7, 26, and 45,

Muller discloses a method and system for queuing packets identified by data flow to be collectively processed that covers all limitations of the parent claims.

Mullers shows that the DMA 120 arranges the packets during processing in memory (Col. 56, lines 30-50; claim 7/26/45 – on-board memory for storage of packets during processing is arranged in packet pages; claim 7/26/45 – packet identifier is an address identifying the beginning of a packet page where data is stored).

- In regards to Claims 9, 28, and 47,

Muller discloses a method and system for queuing packets identified by data flow to be collectively processed that covers all limitations of the parent claims.

Muller shows that the priority for arriving packets may be determined and used to enqueue the packet (Col. 50, lines 25-42; claim 9/28/47 – insertion logic determines a priority and inserts the packet into a particular queue based on the priority).

- In regards to Claims 15, 16, 34, 35, 53, and 54,

Muller discloses a method and system for queuing packets identified by data flow to be collectively processed that covers all limitations of the parent claims.

Through use of batching module 122, flow database 110 and FDM 108 of Fig. 1A, Muller shows that multiple flows of data may be processed using separate data structures (registers) associated with the individual flows (Fig. 5 & 21; Col. 10, lines 42-56; Col. 23-25, lines 30-56; claim 15/34/53 – data packet processor is a multi-streaming processor having separate contexts implemented by registers and associated with individual streams; claim 15/34/53 – selection system causes header information from a packet with a selected identifier to be loaded into an available context; claim 16/35/54 – more contexts than streams).

Muller shows that header information from the arriving packet is loaded into the flow database mechanism in parallel with processing of the packet data (Fig. 1B; Col.

10, lines 42-56; Col. 49, lines 65-67; claim 16/35/54 – loading of header information into available contexts is accomplished in parallel with processing of packets).

- In regards to Claims 18, 37, and 56,

Muller discloses a method and system for queuing packets identified by data flow to be collectively processed that covers all limitations of the parent claims.

Muller shows that the flow database 110, FDM 108 and batching module 122 enable the packets processed and enqueued based on their associated flow (Col. 54-55, lines 47-15; claim 18/37/56 – insertion logic inserts packets into queues at least in part according to flow)

The flow database maintains a flow sequence number for preserving the flow's packet order (Fig. 5; claim 18/37/56 – insertion and selection logic preserve order of packets in individual flows)

- In regards to Claim 58 and 59,

Muller discloses a system of numbering packets in a data processor having a queuing system.

Referring to Figs. 1A & B, 5, and 6A-E, Muller shows that arriving packets are assigned a flow number based on its associated data flow by Header Parser 106, Flow database 110 and FDM 108 (Col. 8-9, lines 50-40).

The flow database 110 can store a fixed amount of flows, which may be re-assigned to newly arriving packets as current packet flows are selected for processing (Col. 35, lines 39-8; Col. 37, lines 9-16; Col. 38, lines 9-22; claim 58 – a packet numbering system having a fixed range of packet numbers, and an assignment facility which marks numbers invalid as packets are sent to be processed and reassigning invalid numbers to newly arrived packets; claim 59 – probe bit associated with each packet ensures the packet number assigned at one time is assigned to the same packet at another time; claim 59 – probe bit is de-asserted when a packet number is assigned and asserted by a Probe and Set command performed by a stream such, after the probe bit is asserted, the asserted probe bit will indicate that the packet number is associated with the same packet).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 2, 3, 5, 19, 21, 22, 24, 38, 40, 41, 43, and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller.

- In regards to Claims 2, 5, 21, 24, 40, and 43,

Muller discloses a method and system for queuing packets identified by data flow to be collectively processed that covers all limitations of the parent claims.

Muller does not explicitly show the number of clusters and queues per cluster varying from 1 to a same maximum such that when the clusters equal 1 the number of queues is the maximum number and vice-versa. Muller also does not explicitly show the maximum number of clusters to be 32 and controlled to be a power of 2.

Muller shows a processor in a preferred embodiment that may store up to a fixed number of packet identifiers (Figs. 8 & 9; claim 2/21/40 - total number of packet identifiers in all queues is fixed) and may use multiple queues for multiple priority levels (Col. 50, lines 25-42). Muller does not explicitly limit the maximum number of queues and clusters that may be used to store data (claim 2/21/40 – the number of clusters and the number of queues per cluster may vary from 1 to a same maximum number such that with the number of clusters equal one the number of queues is the maximum number and vice-versa; claim 5/24/43 – maximum number of either clusters or queues is 32, controlled to be a power of 2)

It would have been obvious to one skilled in the art at the time of the invention to limit the total number of packet identifiers, clusters, and queues to a maximum number depending on the capacity and environment of a particular processor. The Applicant has not disclosed that the number of clusters and queues per cluster varying from 1 to the same maximum provides an advantage or solves a particular problem. One of ordinary skill in the art would have expected the invention to perform equally well with a

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different cluster and queue arrangement. Furthermore, it would have been obvious to one of ordinary skill in the art at the time of the invention to control the number of clusters/queues to be a power of 2, because using powers of 2 enables simple configuration within such a digital/binary environment.

- In regards to Claims 3, 22, and 41,

Muller discloses a method and system for queuing packets identified by data flow to be collectively processed that covers all limitations of the parent claims.

Muller shows that the number of queue groupings may be determined based on the number of different flows set into the flow database register (Col. 9, lines 18-36; Col. 54, lines 47-65; claim 3/22/41 – the relative number of clusters, determining the number of queues, is set by setting a configuration register associated with the processor).

- In regards to Claims 19, 38, and 57,

Muller discloses a method and system for queuing packets identified by data flow to be collectively processed that covers all limitations of the parent claims.

Muller discloses using multiple queues for multiple priority levels but does not explicitly show which priority level is assigned to packets from various locations.

Priority may be assigned to packets based on a variety of criteria. Assignment of priority is arbitrary and is based on the specific purpose of the processor and the

environment in which it is operating (claim 19/38/57 – insertion logic treats packets from network/switching fabric with highest priority, packet identifiers for requeuing with the next highest priority, packet identifiers generated by software with a lowest priority).

It would have been obvious to one skilled in the art at the time of the invention to assign priority levels to packets based on the implementation considerations of the particular processor. The Applicant has not disclosed that the assignment of priority to any one type of packet provides an advantage or solves a particular problem. One of ordinary skill in the art would have expected the invention to perform equally well with a different priority arrangement.

9. Claims 10, 13, 14, 29, 32, 33, 48, 51, and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller in view of Tzeng (US006438135B1).

- In regards to Claims 10, 13, 14, 29, 32, 33, 48, 51, and 52,

Muller discloses a method and system for queuing packets identified by data flow to be collectively processed that covers all limitations of the parent claims.

Muller discloses using multiple queues for multiple priority levels but does not explicitly show numbering queue cluster and prioritizing processing by cluster number. Muller also does not explicitly show how packets are selected from queues based on priority.

Tzeng discloses a queuing switch and method for processing data packets transmitted through a network (Abstract). Referring to Fig. 1-5, Tzeng shows an incoming packet processor 18 that creates an identifier EID for each incoming packet, assigns numbers to priority queues for storing the packets based on the created EID (claim 10/29/48 – clusters are numbered and priority for processing identified packets is by cluster number), and selects the packet from the queues based on the priority queue number (Col. 3, lines 48-50; claim 13/32/51 – selection system selects packets for processing based upon priority by queue number). Tzeng further discloses a weighted round robin technique for processing the various queues (Col. 5, lines 27-60; claim 14/33/52 – fairness algorithm is followed in selecting a queue within a priority cluster for selecting a packet for processing).

It would have obvious to one of ordinary skill in the art at the time of the invention to adapt the method and system of Muller by providing a number priority to cluster of queues for storing packets of multiple priority levels and selecting packets for processing based on the queue priorities using a fairness algorithm, as taught by Tzeng. This modification enables efficient storage and processing of data packets having different formats, protocols, and quality of service requirements.

Allowable Subject Matter

10. Claims 8, 11, 12, 17, 27, 30, 31, 36, 46, 49, 50, and 55 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in

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independent form including all of the limitations of the base claim and any intervening claims.

- In regards to Claims 8, 27, and 46,

Muller discloses a method and system for queuing packets identified by data flow to be collectively processed that covers all limitations of the parent claims.

Muller shows that the packet identifiers may comprise information on the source and/or destination of the packet (Col. 7, lines 30-50).

However, neither Muller nor the prior art of record shows created and queued packet identifiers that comprise the identifier of the source device as well as an indication of whether the packet has increased or decreased in total size during processing, an indication of whether or not processing is completed on that packet, a next queue into which the packet identifier should be inserted, and an identifier of whether the packet is being currently being processed.

- Claims 11, 12, 17, 30, 31, 36, 49, 50, and 55 depend from claims 8, 27, and 46, respectively.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.


- Zaun et al. (US 20010024456A1) discloses an MPEG re-multiplexer having multiple inputs and multiple outputs
- Doshi et al. (US006219339B1) discloses a method and apparatus for selectively discarding packets
- Narad et al. (US006157955A) discloses a packet processing system including a policy engine having a classification unit
- Hansen et al. (US005809321A) discloses a general purpose, multiple precision parallel operation, programmable media processor
- Picazo, Jr. et al. (US005737525A) discloses a network packet switch using shard memory for repeating and bridging packets at media rate
- Gallagher et al. (US005619497A) discloses a method and apparatus for reordering frames
- Choudhury et al. (US005521916A) discloses an implementation of selective pushout for space priorities in a shared memory asynchronous transfer mode switch
- Yang et al. (US005465331A) discloses an apparatus having three separated and decentralized processors for concurrently and independently processing packets in a communication network

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gregory B Sefcheck whose telephone number is 703-305-0633. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on 703-305-4744. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GBS
3-26-2004



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